

CLAIMS

What is claimed is:

1 1. A high speed interconnection link that comprises:
2 a receiver configured to receive a plurality of channels;
3 a receiver logic circuit configured to receive signals from each of the plurality of channels
4 and monitor the signals for symbols that are unique to each channel, wherein upon detecting
5 unexpected symbols in the channels, the receiver logic circuit is configured to correct the order of
6 the channels.

1 2. The link of claim 1, further comprising a transmitter coupled to the plurality of channels
2 and a transmitter logic circuit configured to transmit signals to corresponding channels, wherein
3 the transmitter logic circuit is configured to reorder the correspondence of the signals transmitted
4 to the channels.

1 3. The link of claim 2, wherein the transmitter logic circuit comprises a bank of multiplexers
2 each configured to transmit a selected one of two input signals to be transmitted through a channel.

1 4. The link of claim 1, wherein the receiver logic circuit comprises a bank of multiplexers
2 each configured to transmit a selected one of two input signals received from a channel.

1 5. The link of claim 1, wherein the receiver logic circuit comprises a bank of multiplexers
2 each configured to transmit a selected one of all the signals received in the channels.

6 a transmit port comprising a lane reorder circuit that is configured to reroute the channel
7 signals if the transmit port does not detect a predetermined response from the receiver port.

1 12. The method of claim 11, wherein the order of the data signals is corrected during the
2 transmission of a first and a second set of training data, the training data comprising a
3 predetermined sequence of binary words that are transmitted through each channel in the link,
4 wherein at least one of the binary words transmitted through each channel is a unique lane
5 identifier.

1 13. The method of claim 12 wherein said transmitting includes:
2 the transmitter port transmitting the first set of training data to the receiver port;
3 the receiver port transmitting the first set of training data to the transmitter port if the
4 receiver port receives the first set of training data;
5 the transmitter port transmitting the second set of training data to the receiver port if the
6 transmitter port successfully detects a set of training data from the receiver port; and
7 the receiver port transmitting the second set of training data to the transmitter port if the
8 receiver port successfully detects a set of training data;
9 wherein once both ports are transmitting and receiving the second set of training data,
10 correction of the order of data signals in the channels is complete and the link is properly
11 configured to transmit data.

1 ~~14.~~ A computer network that comprises:
2 a first device having a first adapter;

